BY DRAFTSMAN CLASS SUBCLASS

Provide SOI wafer, 101 deposit etch stop layers, deposit mandrel layer 116 Pattern gate materials Pattern mandrel layer; 102 form sidewall spacer, pattern etch stop layers 100 Form source/drain and 118 halo implants Pattern SOI layer, form 104 gate oxide Deposit dielectric, 120 planerize and recess Deposit and planerize 106 gate material Form sidewall spacers 122 on gates, etch dielectric Pattern remaining mandrel layer; pattern 108 etching layer Form contacts 124 110 Pattern SOI layer Complete transistors 126 Deposit and planerize 112 gate material

FIG. 1

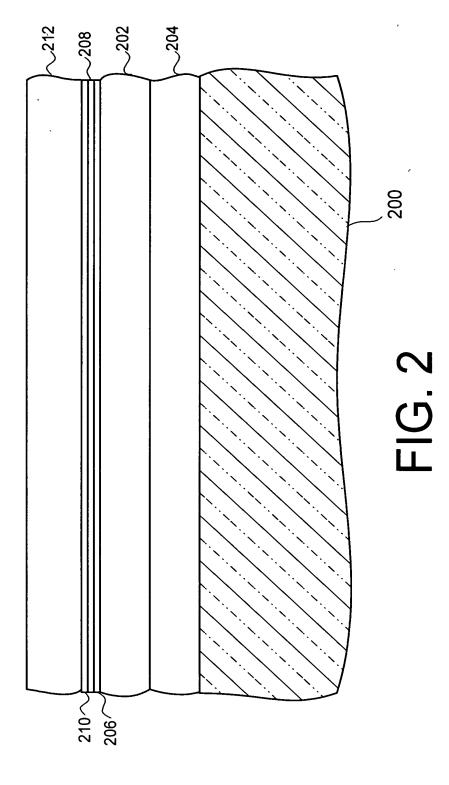
114

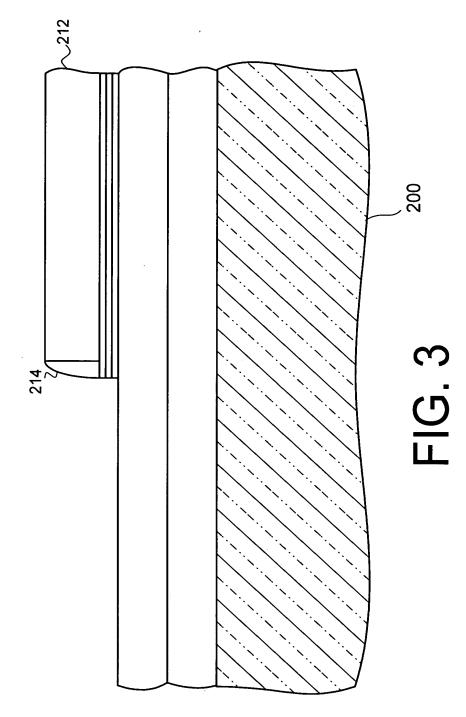
Remove sidewall spacer;

fill with polysilicon

APPROVED O.G. FIG.

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O988823.O62101

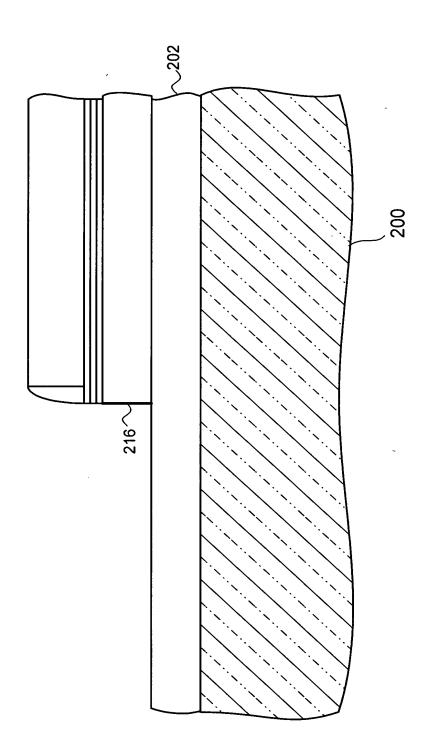


FIG. 4

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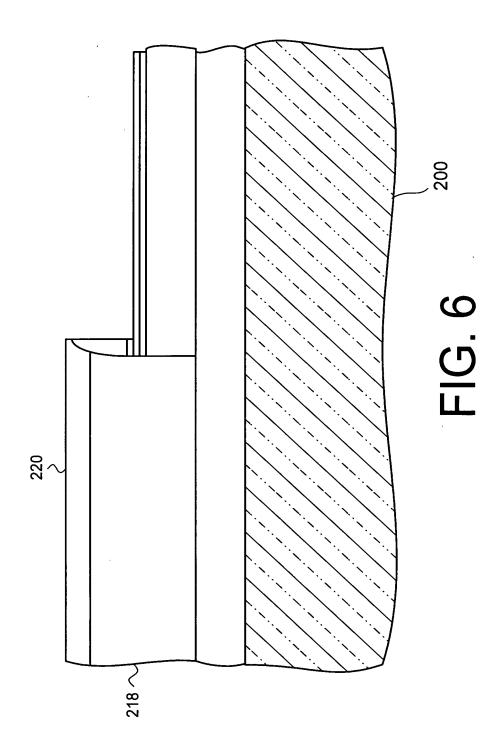
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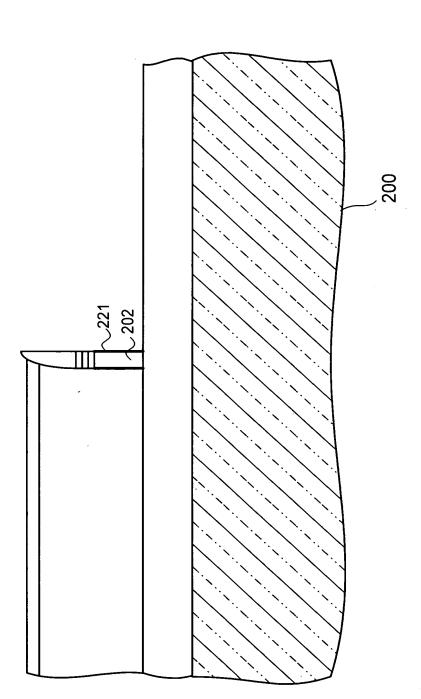
FIG. 5

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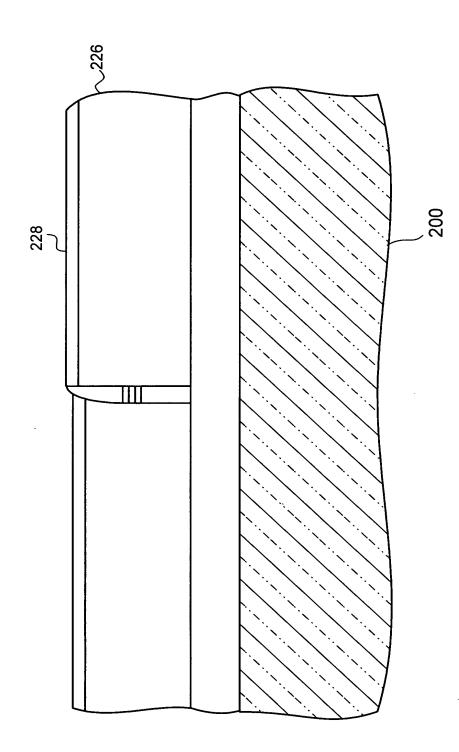
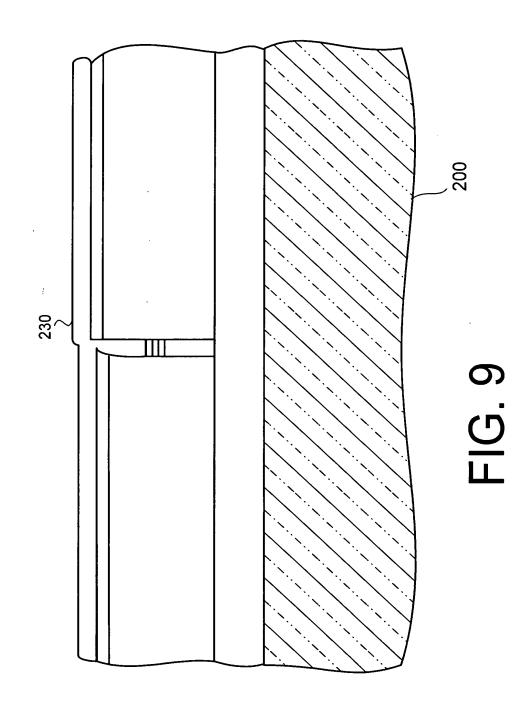
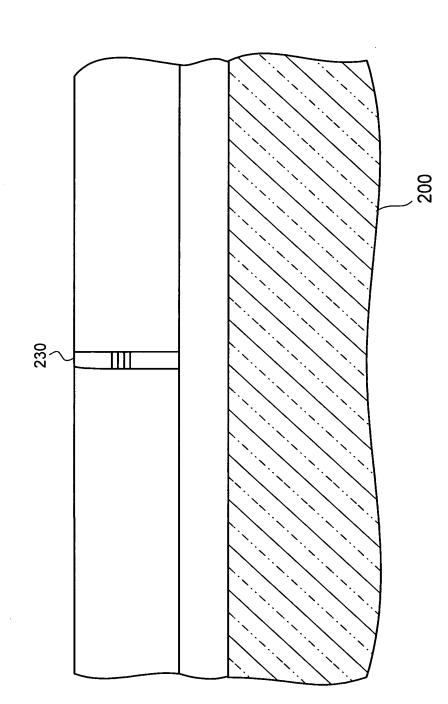


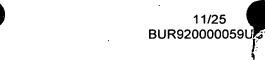
FIG. 8

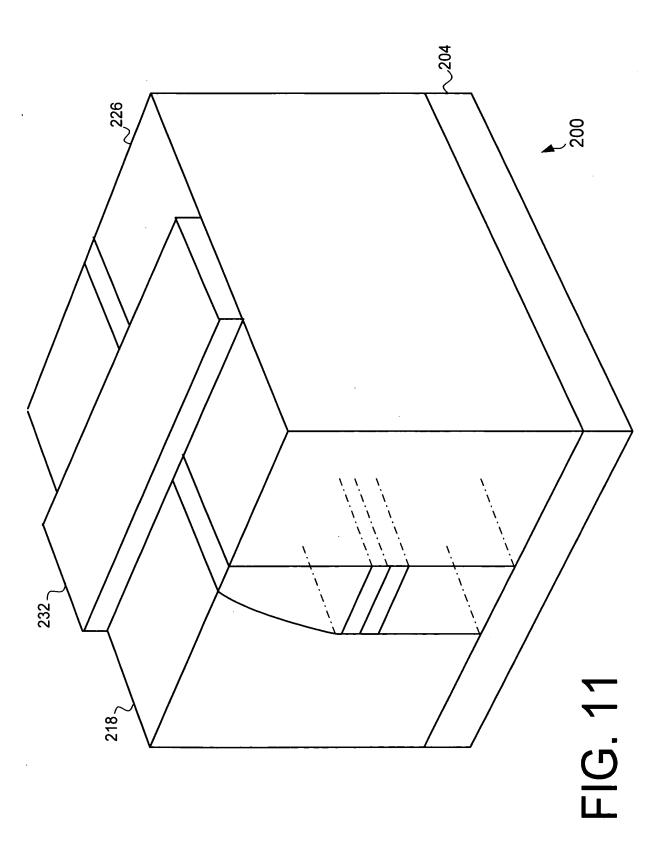






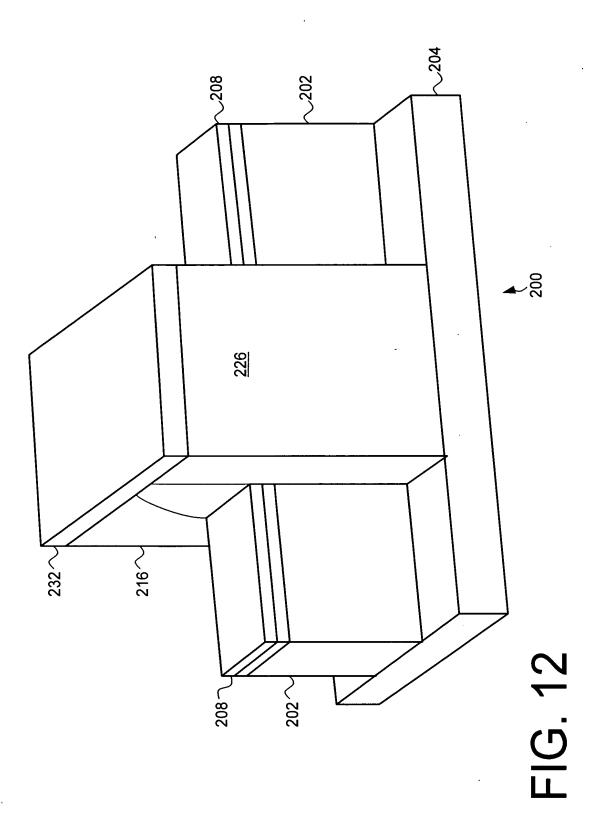
Desesell ostaci

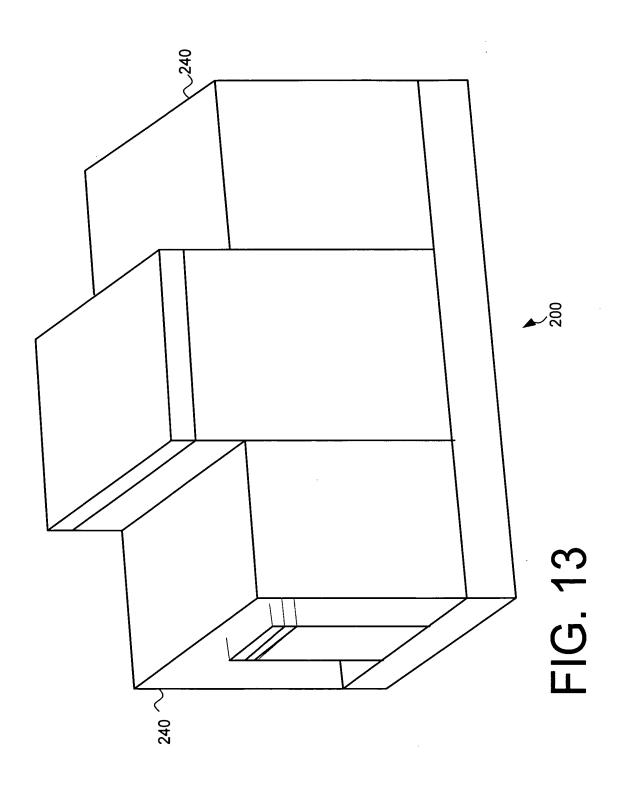


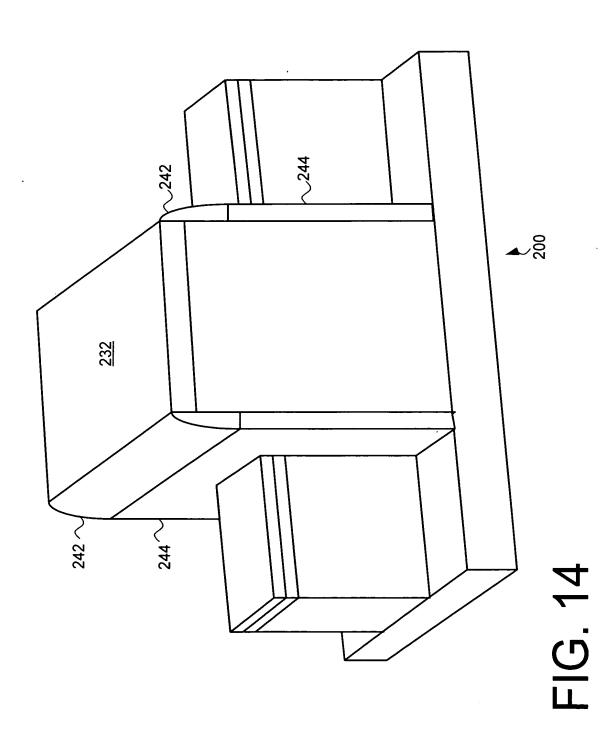


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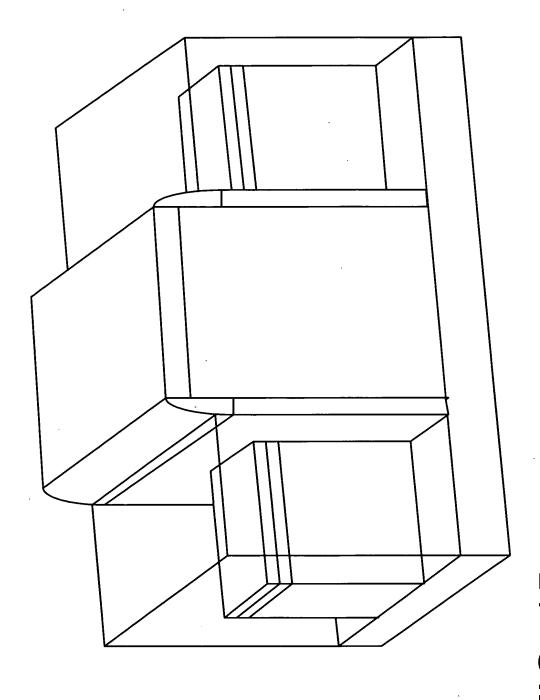
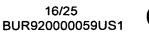


FIG. 15



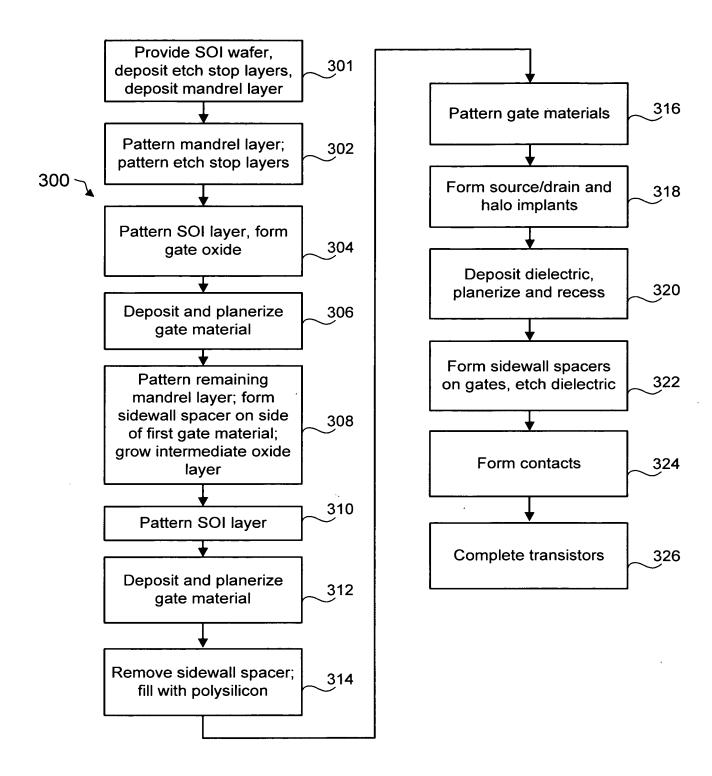


FIG. 16

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APPROVED O.G. FIG.

CLASS SUBCLASS вч DRAFTSMAN

> 200 FIG. 17

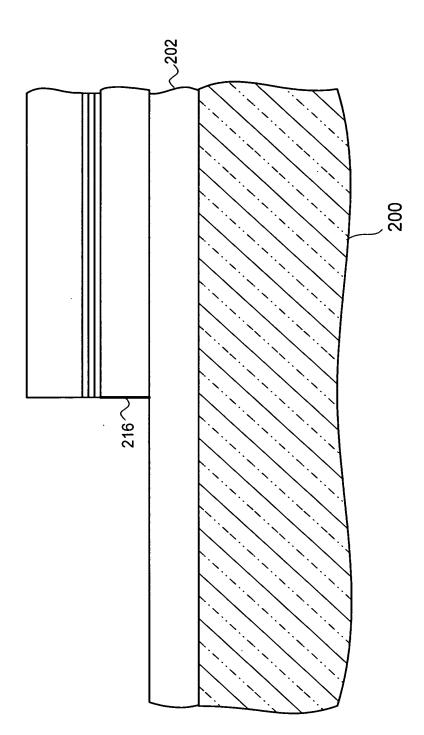
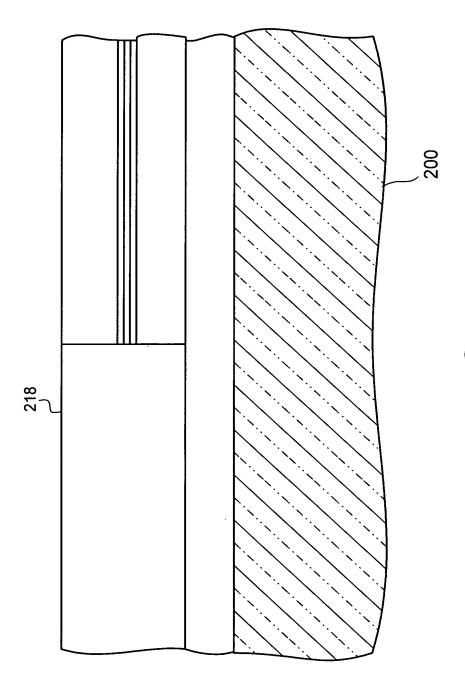
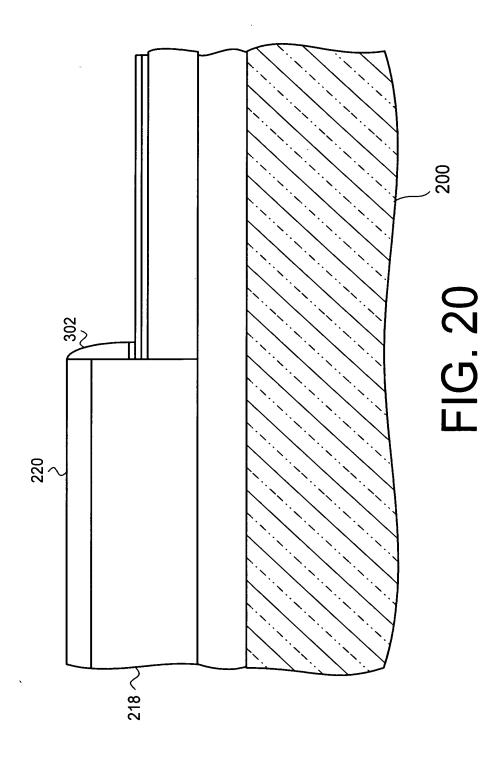


FIG. 18



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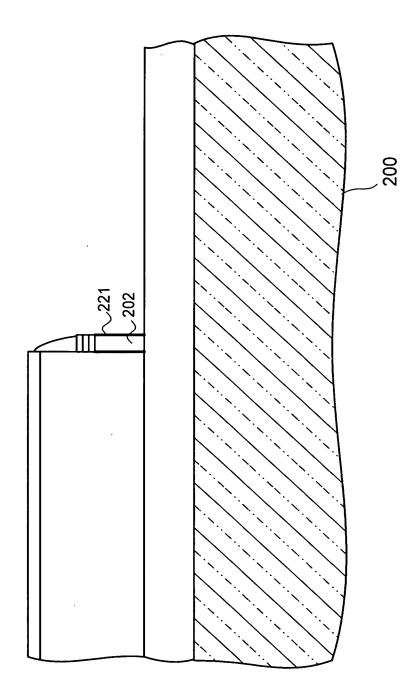
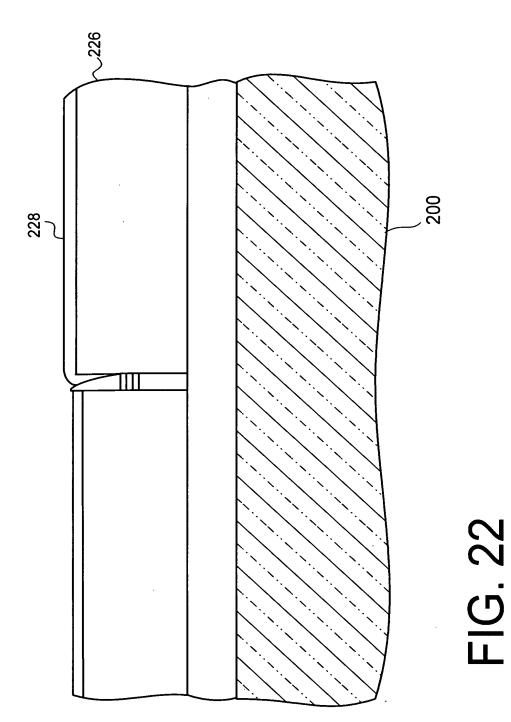


FIG. 21





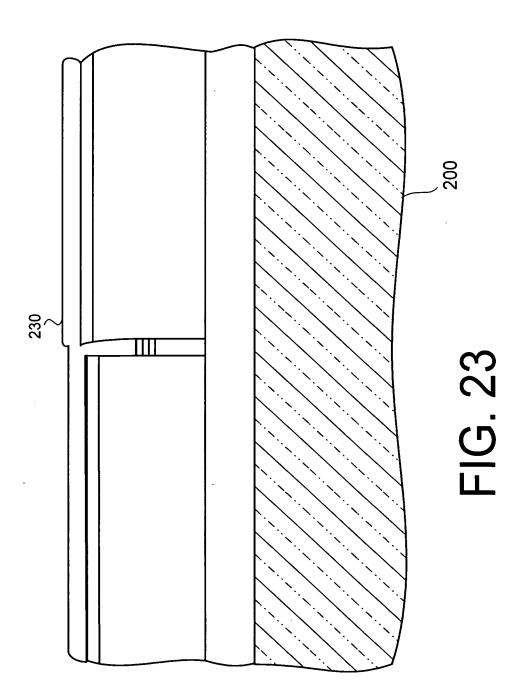
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APPROVED O.G. FIG.

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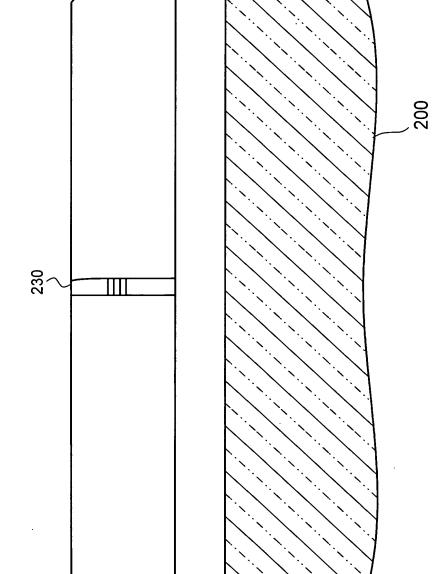
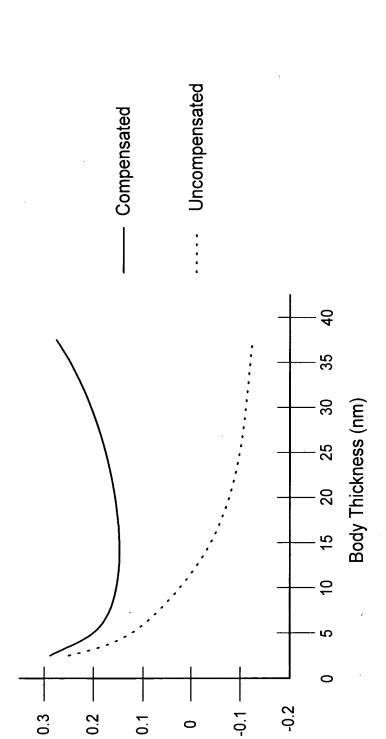


FIG. 24

APPROVED O.G. FIG.
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Threshold Voltage (V)

FIG. 25